WESTERN DIGITAL
CORPORATION

WD1943(8116)/WD1945(8136) Dual Baud Rate Clock

FEATURES

- 16 SELECTABLE BAUD RATE CLOCK FREQUENCIES
- OPERATES WITH CRYSTAL OSCILLATOR OR EXTERNALLY GENERATED FREQUENCY INPUT
- ROM MASKABLE FOR NON-STANDARD FREQUENCY SELECTIONS
- INTERFACES EASILY WITH MICROCOMPUTERS
- OUTPUTS A 50% DUTY CYCLE CLOCK WITH 0.01% ACCURACY
- 6 DIFFERENT FREQUENCY/DIVISOR PAIRS AVAILABLE
- SINGLE +5V POWER SUPPLY
- COMPATIBLE WITH BR1941
- TTL, MOS COMPATIBILITY

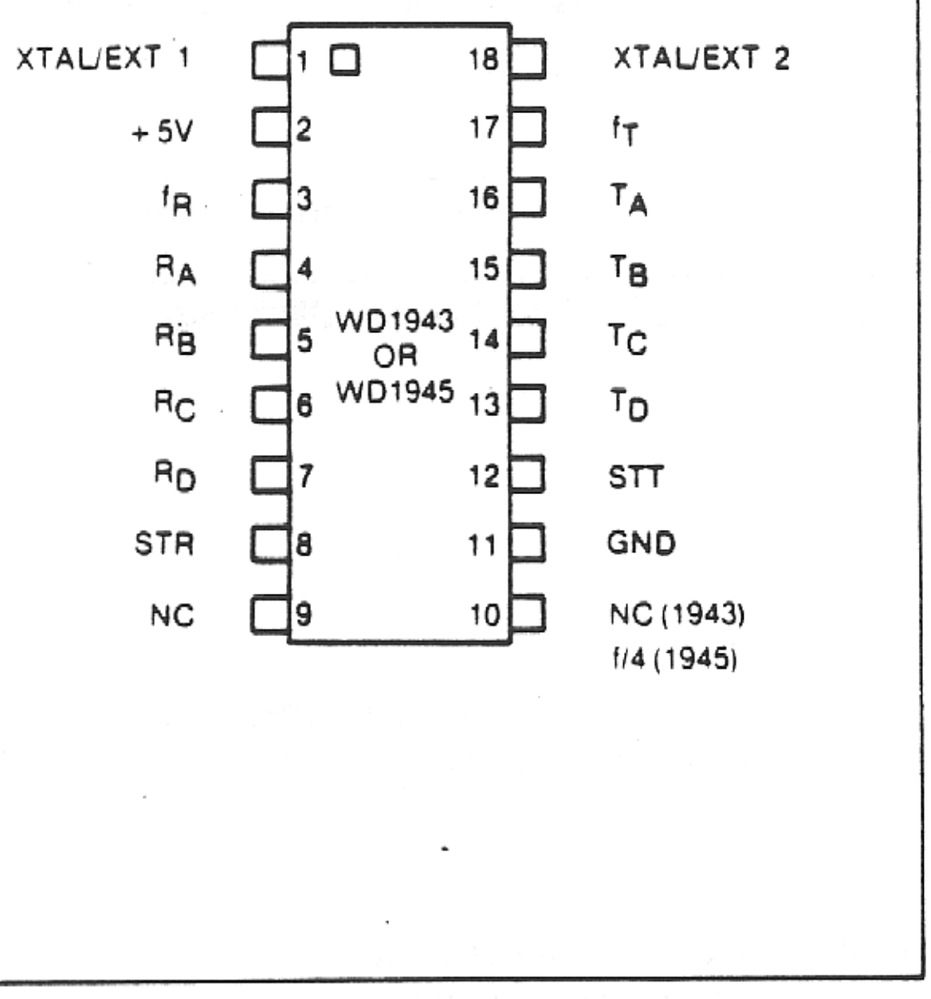
- WD1943 IS PIN COMPATIBLE TO THE COM8116
- WD1945 IS PIN COMPATIBLE TO THE COM8136 AND COM5036 (PIN 9 ON WD1945 IS A NO CONNECT)

GENERAL DESCRIPTION

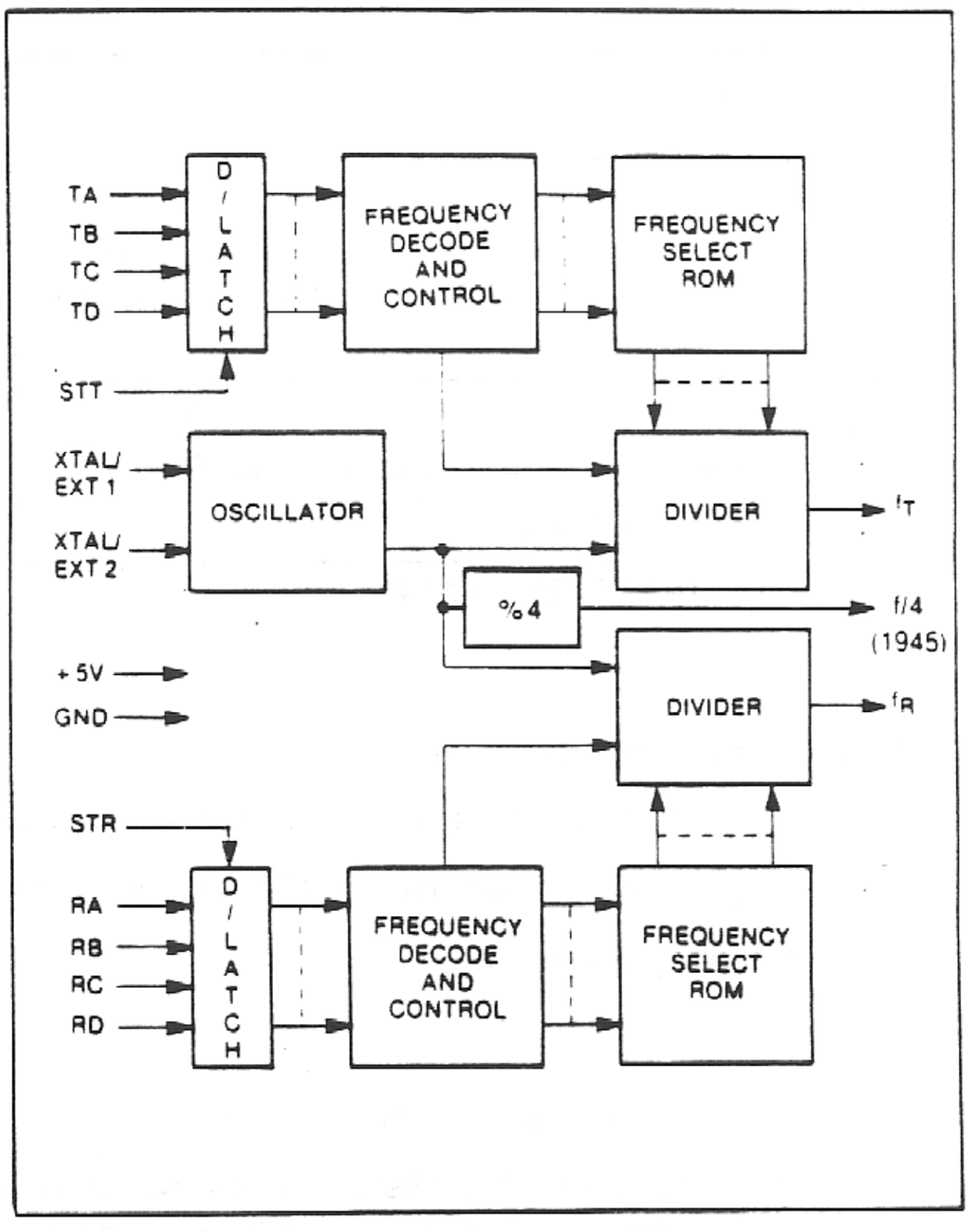
The WD1943/45 is an enhanced version of the BR1941 Dual Baud Rate Clock. The WD1943/45 is a combination Baud Rate Clock Generator and Programmable Divider. It is manufactured in N-channel MOS using silicon gate technology. This device is capable of generating 16 externally selected clock rates whose frequency is determined by either a single crystal or an externally generated input clock. The WD1943/45 is a programmable counter capable of generating a division by any integer from 4 to $2^{15} - 1$, inclusive.

The WD1943/45 is available programmed with the most used frequencies in data communication. Each frequency is selectable by strobing or hard wiring each of the two sets of four Rate Select inputs. Other frequencies/division rates can be generated by reprogramming the internal ROM coding through a MOS mask change. Additionally, further clock division may be accomplished through cascading of devices. The frequency output is fed into the XTAL/EXT input on a subsequent device.

The WD1943/45 can be driven by an external crystal or by TTL logic.



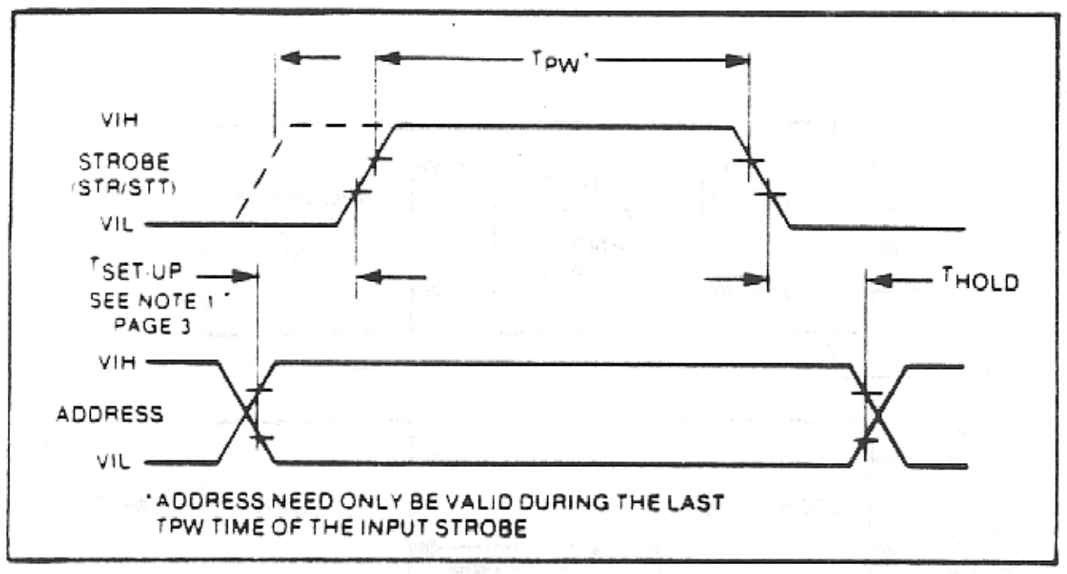
PIN CONNECTIONS



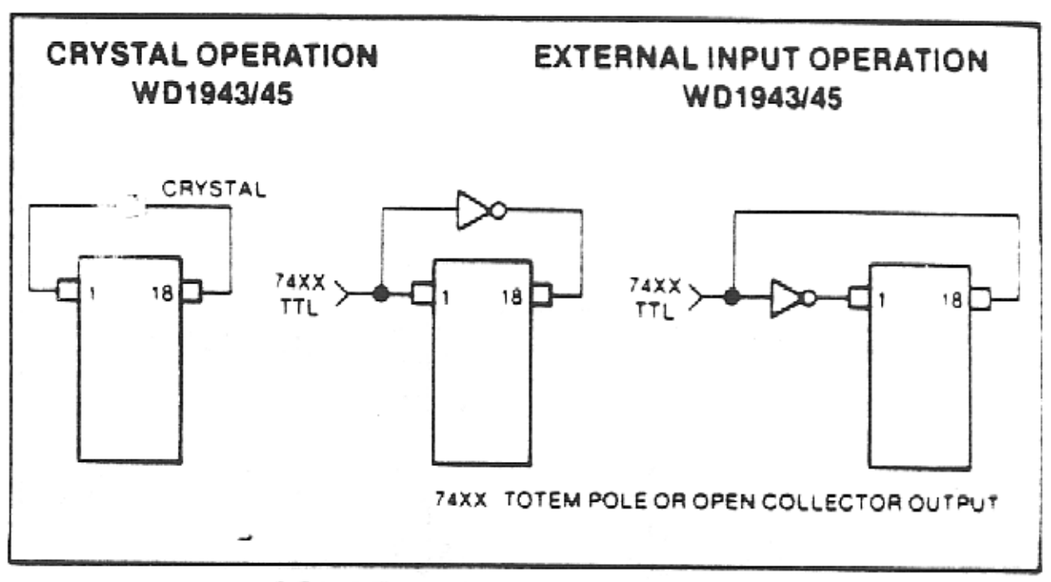
BLOCK DIAGRAM

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME	FUNCTION
1	XTAL/EXT 1	Crystal or External Input 1	This input receives one pin of the crystal package or one polarity of the external input.
2	V_{CC}	Power Supply	+ 5 volt Supply
3	f_R	Receiver Output Frequency	This output runs at a frequency selected by the Receiver Address inputs.
4-7	R_A, R_B, R_C, R_D	Receiver Address	The logic level on these inputs as shown in Table 1 thru 6, selects the receiver output frequency, f_R.
8	STR	Strobe-Receiver Address	A high-level input strobe loads the receiver address (R_A, R_B, R_C, R_D) into the receiver address register. This input may be strobed or hard wired to + 5V.
9	NC	No Connection	No Internal Connection
10	NC (1943) f/4 (1945)	No Connection freq/4 Output	No Internal Connection XTAL1 input freq divided by four.
11	GND	Ground	Ground
12	STT	Strobe-Transmitter Address	A high-level input strobe loads the transmitter address (T_A, T_B, T_C, T_D) into the transmitter address register. This input may be strobed or hard wired to + 5V.
13-16	T_D, T_C, T_B, T_A	Transmitter Address	The logic level on these inputs, as shown in Table 1 thru 6, selects the transmitter output frequency, f_T.
17	f_T	Transmitter Output Frequency	This output runs at a frequency selected by the Transmitter Address inputs.
18	XTAL/EXT 2	Crystal or External Input 2	This input receives the other pin of the crystal package or the other polarity of the external input.



CONTROL TIMING



CRYSTAL/CLOCK OPTIONS

ABSOLUTE MAXIMUM RATINGS

Positive Voltage on any Pin, with respect to ground	+ 7.0V
Negative Voltage on any Pin, with respect to ground	– 0.3V
Storage Temperature (plastic package)	– 55°C to + 125°C
(Cerdip package and Ceramic package)	– 65°C to + 150°C
Lead Temperature (Soldering, 10 sec.)	+ 325°C

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and Functional Operation of the device at these or at any other condition above those indicated in the operational sections of this specification are not implied.

ELECTRICAL CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = +5V ±5% standard.)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
DC CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low-level, V_{IL}			0.8	V	See Note 1
High-level, V_{IH}	2.0		V_{CC}	V	
OUTPUT VOLTAGE LEVELS					
Low-level, V_{OL}			0.4	V	I_{OL} = 3.2 mA
High-level, V_{OH}	V_{CC}-1.5	4.0		V	I_{OH} = 100µA
INPUT CURRENT					
High-level, I_{IH}			– 10	µA	$V_{IN} = V_{CC}$ } STR (8) and STT (12) Only
Low-level, I_{IL}			10	µA	V_{IN} = GND } STR (8) and STT (12) Only
Low-level, I_{IL}			300	µA	V_{IN} = GND (All inputs except XTAL, STR and STT)
INPUT CAPACITANCE					
All Inputs, C_{IN}		5	10	pf	V_{IN} = GND, excluding XTAL inputs
EXT. INPUT LOAD		4	5		Series 7400 unit loads
INPUT RESISTANCE					
Crystal Input, R_{XTAL}	1.1			KΩ	Resistance to ground for Pin 1 and Pin 18
POWER SUPPLY CURRENT					
I_{CC}		40	80	mA	
AC CHARACTERISTICS					T_A = +25°C
CLOCK FREQUENCY					See Note 2
PULSE WIDTH (T_{PW})					
Clock					50% Duty Cycle ± 10%. See Note 2
Receiver strobe	150		DC	ns	See Note 3
Transmitter strobe	150		DC	ns	See Note 3
INPUT SET-UP TIME (T_{SET-UP})					
Address	50			ns	See Note 3
OUTPUT HOLD TIME (T_{HOLD})					
Address	50			ns	
STROBE TO NEW FREQUENCY DELAY			6	CLK	

NOTE 1: XTAL/EXT inputs are either TTL compatible or crystal compatible. See crystal specification in Applications Information section.
All inputs except XTAL, STR and STT have internal pull-up resistors.

NOTE 2: Refer to frequency option tables for maximum input frequency on XTAL/EXT pins.
Typical clock pulse width is 1/2 x CL

NOTE 3: Input set-up time can be decreased to >0 ns by increasing the minimum strobe width (50 ns) to a total of 200 ns.
T_{A-D} and R_{A-D} have internal pull-up resistors.

OPERATION

Standard Frequencies

Choose a Transmitter and Receiver frequency from the table below. Program the corresponding address into TA-TD and RA-RD respectively using strobe pulses or by hard wiring the strobe and address inputs.

Non-Standard Frequencies

To accomplish non-standard frequencies do one of the following:

1. Choose a crystal that when divided by the WD1943 generates the desired frequency.
2. Cascade devices by using the frequency outputs as an input to the XTAL/EXT inputs of the subsequent WD1943/45.
3. Consult the factory for possible changes via ROM mask reprogramming.

FREQUENCY OPTIONS

TABLE 1. CRYSTAL FREQUENCY = 5.0688 MHZ

Transmit/Receive Address				Baud Rate (16X Clock)	Theoretical Freq. (kHz)	Actual Freq. (kHz)	Percent Error	Duty Cycle %	Divisor
D	C	B	A						
0	0	0	0	50	0.8	0.8	—	50/50	6336
0	0	0	1	75	1.2	1.2	—	50/50	4224
0	0	1	0	110	1.76	1.76	—	50/50	2880
0	0	1	1	134.5	2.152	2.1523	0.016	50/50	2355
0	1	0	0	150	2.4	2.4	—	50/50	2112
0	1	0	1	300	4.8	4.8	—	50/50	1056
0	1	1	0	600	9.6	9.6	—	50/50	528
0	1	1	1	1200	19.2	19.2	—	50/50	264
1	0	0	0	1800	28.8	28.8	—	50/50	176
1	0	0	1	2000	32.0	32.081	0.253	50/50	158
1	0	1	0	2400	38.4	38.4	—	50/50	132
1	0	1	1	3600	57.6	57.6	—	50/50	88
1	1	0	0	4800	76.8	76.8	—	50/50	66
1	1	0	1	7200	115.2	115.2	—	50/50	44
1	1	1	0	9600	153.6	153.6	—	48/52	33
1	1	1	1	19,200	307.2	316.8	3.125	50/50	16

WD1943-00 or WD1945-00

TABLE 2. CLOCK FREQUENCY = 2.76480 MHZ

Transmit/Receive Address				Baud Rate (16X Clock)	Theoretical Freq. (kHz)	Actual Freq. (kHz)	Percent Error	Duty Cycle %	Divisor
D	C	B	A						
0	0	0	0	50	0.8	0.8	—	50/50	3456
0	0	0	1	75	1.2	1.2	—	50/50	2304
0	0	1	0	110	1.76	1.76	– 0.006	50/50	1571
0	0	1	1	134.5	2.152	2.152	– 0.019	50/50	1285
0	1	0	0	150	2.4	2.4	—	50/50	1152
0	1	0	1	200	3.2	3.2	—	50/50	864
0	1	1	0	300	4.8	4.8	—	50/50	576
0	1	1	1	600	9.6	9.6	—	50/50	288
1	0	0	0	1200	19.2	19.2	—	50/50	144
1	0	0	1	1800	28.8	28.8	—	50/50	96
1	0	1	0	2000	32.0	32.15	+ 0.465	50/50	86
1	0	1	1	2400	38.4	38.4	—	50/50	72
1	1	0	0	3600	57.6	57.6	—	50/50	48
1	1	0	1	4800	76.8	76.8	—	50/50	36
1	1	1	0	9600	153.6	153.6	—	50/50	18
1	1	1	1	19,200	307.2	307.2	—	50/50	9

WD1943-02 or WD1945-02

TABLE 3. CRYSTAL FREQUENCY = 6.018305 MHZ

Transmit/Receive Address				Baud Rate (16X Clock)	Theoretical Freq. (kHz)	Actual Freq. (kHz)	Percent Error	Duty Cycle %	Divisor
D	C	B	A						
0	0	0	0	50	0.8	.7999	0	50/50	7523*
0	0	0	1	75	1.2	1.2000	0	50/50	5015*
0	0	1	0	110	1.76	1.7597	0	50/50	3420
0	0	1	1	134.5	2.152	2.1517	0	50/50	2797*
0	1	0	0	150	2.4	2.3996	0	50/50	2508
0	1	0	1	200	3.2	3.1995	0	50/50	1881*
0	1	1	0	300	4.8	4.7993	0	50/50	1254
0	1	1	1	600	9.6	9.5986	0	50/50	627*
1	0	0	0	1200	19.2	19.2279	+ 0.14	50/50	31.3*
1	0	0	1	1800	28.8	28.7959	0	50/50	209*
1	0	1	0	2000	32.0	32.0125	0	50/50	188
1	0	1	1	2400	38.4	38.3334	– 0.17	50/50	157*
1	1	0	0	3600	57.6	57.8687	+ 0.46	50/50	104
1	1	0	1	4800	76.8	77.1583	+ 0.46	50/50	78
1	1	1	0	9800	153.6	154.3166	+ 0.46	50/50	39*
1	1	1	1	19,200	307.2	300.9175	– 2.04	50/50	20

WD1943-03 or WD1945-03

TABLE 4. CLOCK FREQUENCY = 5.52960 MHZ

Transmit/Receive Address				Baud Rate (32X Clock)	Theoretical Freq. (kHz)	Actual Freq. (kHz)	Percent Error	Duty Cycle %	Divisor
D	C	B	A						
0	0	0	0	50	1.6	1.6	—	50/50	3456
0	0	0	1	75	2.4	2.4	—	50/50	2304
0	0	1	0	110	3.52	3.52	—	50/50	1571
0	0	1	1	134.5	4.304	4.303	– 0.006	50/50	1285
0	1	0	0	150	4.8	4.8	– 0.019	50/50	1152
0	1	0	1	200	6.4	6.4	—	50/50	864
0	1	1	0	300	9.6	9.6	—	50/50	576
0	1	1	1	600	19.2	19.2	—	50/50	288
1	0	0	0	1200	38.4	38.4	—	50/50	144
1	0	0	1	1800	57.6	57.6	—	50/50	96
1	0	1	0	2000	64.0	64.3	+ 0.465	50/50	86
1	0	1	1	2400	76.8	76.8	—	50/50	72
1	1	0	0	3600	115.2	115.2	—	50/50	48
1	1	0	1	4800	153.6	153.6	—	50/50	36
1	1	1	0	9600	307.2	307.2	—	50/50	18
1	1	1	1	19,200	614.4	614.4	—	50/50	9

WD1943-04 or WD1945-04

TABLE 5. CRYSTAL FREQUENCY = 4.9152 MHZ

Transmit/Receive Address				Baud Rate (16X Clock)	Theoretical Freq. (kHz)	Actual Freq. (kHz)	Percent Error	Duty Cycle %	Divisor
D	C	B	A						
0	0	0	0	50	0.8	0.8	—	50/50	6144
0	0	0	1	75	1.2	1.2	—	50/50	4096
0	0	1	0	110	1.76	1.7598	– 0.01	*	2793
0	0	1	1	134.5	2.152	2.152	—	50/50	2284
0	1	0	0	150	2.4	2.4	—	50/50	2048
0	1	0	1	300	4.8	4.8	—	50/50	1024
0	1	1	0	600	9.6	9.6	—	50/50	512
0	1	1	1	1200	19.2	19.2	—	50/50	256
1	0	0	0	1800	28.8	28.7438	– 0.19	*	171
1	0	0	1	2000	32.0	31.9168	– 0.26	50/50	154
1	0	1	0	2400	38.4	38.4	—	50/50	128
1	0	1	1	3600	57.6	57.8258	0.39	*	85
1	1	0	0	4800	76.8	76.8	—	50/50	64
1	1	0	1	7200	115.2	114.306	– 0.77	*	43
1	1	1	0	9600	153.6	153.6	—	50/50	32
1	1	1	1	19,200	307.2	307.2	—	50/50	16

WD1943-05 or WD1945-05

TABLE 6. CRYSTAL FREQUENCY = 5.0688 MHZ

Transmit/Receive Address				Baud Rate (32X Clock)	Theoretical Freq. (kHz)	Actual Freq. (kHz)	Percent Error	Duty Cycle %	Divisor
D	C	B	A						
0	0	0	0	50	1.6	1.6	—	50/50	3168
0	0	0	1	75	2.4	2.4	—	50/50	2112
0	0	1	0	110	3.52	3.52	—	50/50	1440
0	0	1	1	134.5	4.304	4.303	.026	50/50	1178
0	1	0	0	150	4.8	4.8	—	50/50	1056
0	1	0	1	200	6.4	6.4	—	50/50	792
0	1	1	0	300	9.6	9.6	—	50/50	528
0	1	1	1	600	19.2	19.2	—	50/50	264
1	0	0	0	1200	38.4	38.4	—	50/50	132
1	0	0	1	1800	57.6	57.6	—	50/50	88
1	0	1	0	2400	76.8	76.8	—	50/50	66
1	0	1	1	3600	115.2	115.2	—	50/50	44
1	1	0	0	4800	153.6	153.6	—	*	33
1	1	0	1	7200	230.4	230.4	—	50/50	22
1	1	1	0	9600	307.2	298.16	2.941	*	17
1	1	1	1	19,200	614.4	633.6	3.125	50/50	8

*When the duty cycle is not exactly 50% it is 50% ± 10%

WD1943-06 or WD1945-06

APPLICATIONS INFORMATION

OPERATION WITH A CRYSTAL

The WD1943/45 Baud Rate Generator may be driven by either a crystal or TTL level clock. When using a crystal, the waveform that appears at pins 1 (XTAL/EXT 1) and 18 (XTAL/EXT 2) does not conform to the normal TTL limits of $V_{IL} \leqslant 0.8V$ and $V_{IH} \geqslant 2.0V$. Figure 1 illustrates a typical crystal waveform when connected to a WD1943/45.

Since the D.C. level of the waveform causes the least positive point to typically be greater than 0.8V, the WD1943/45 is designed to look for an edge, as opposed to a TTL level. The XTAL/EXT logic triggers on a rising edge of typically 1V in magnitude. This allows the use of a crystal without any additional components.

OPERATIONS WITH TTL LEVEL CLOCK

With clock frequencies in the area of 5 MHz, significant overshoot and undershoot ("ringing") can appear at pins 1 and/or 18. The clock oscilator may, at times be triggered on a rising edge of an overshoot or undershoot waveform, causing the device to effectively "double-trigger." This phenomenon may result as a twice expected baud rate, or as an apparent device failure. Figure 2 shows a typical waveform that exhibits the "ringing" problem.

The design methods required to minimize ringing include the following:

1. Minimize the P.C. trace length. At 5 MHz, each inch of trace can add significantly to overshoot and undershoot.
2. Match impedances at both ends of the trace. For example, a series resistor near the device may be helpful.
3. A uniform impedance is important. This can be accomplished through the use of:
   a. parallel ground lines
   b. evenly spaced ground lines crossing the trace on the opposite side of PC board
   c. an inner plane of ground, e.g., as in a four layered PC board.

In the event that ringing exists on an already finished board, several techniques can be used to reduce it. These are:

1. Add a series resistor to match impedance as shown in Figure 3.
2. Add pull-up/pull-down resistor to match impedance, as shown in Figure 4.
3. Add a high speed diode to clamp undershoot, as shown in Figure 5.

The method that is easiest to implement in many systems is method 1, the series resistor. The series resistor will cause the D.C. level to shift up, but that does not cause a problem since the OSC is triggered by an edge, as opposed to a TTL level.

The 1943/45 Baud Rate Generator can save both board space and cost in a communications system. By choosing either a crystal or a TTL level clock, the user can minimize the logic required to provide baud rate clocks in a given design.

POWER LINE SPIKES

Voltage transients on the AC power line may appear on the DC power output. If this possibility exists, it is suggested that a by-pass capacitor is used between +5V and GND.

CRYSTAL SPECIFICATIONS

User must specify termination (pin, wire, other)
Frequency — See Tables 1-6.
Temperature range 0°C to +70°C
Series resistance $\leqslant 50\Omega$
Series resonant
Overall tolerance ± 0.01%

CRYSTAL MANUFACTURERS (Partial List)

American Time Products Div.
Frequency Control Products, Inc.
61-20 Woodside Ave.
Woodside, New York 11377
(213) 458-5811

Bliley Electric Co.
2545 Grandview Blvd.
Erie, Pennsylvania 16508
(814) 838-3571

M-tron Ind. Inc.
P.O. Box 630
Yankton, South Dakota 57078
(605) 665-9321

Erie Frequency Control
453 Lincoln St.
Calisle, Pennsylvania 17013
(714) 249-2232

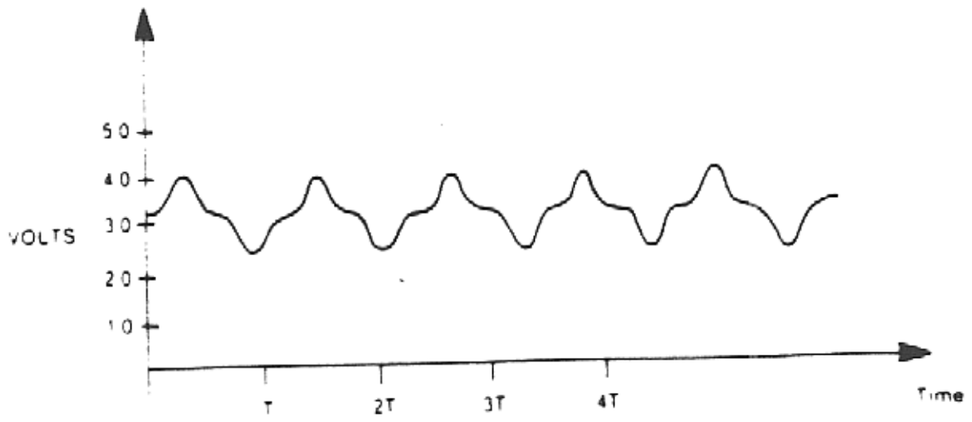


Figure 1. TYPICAL CRYSTAL WAVEFORM

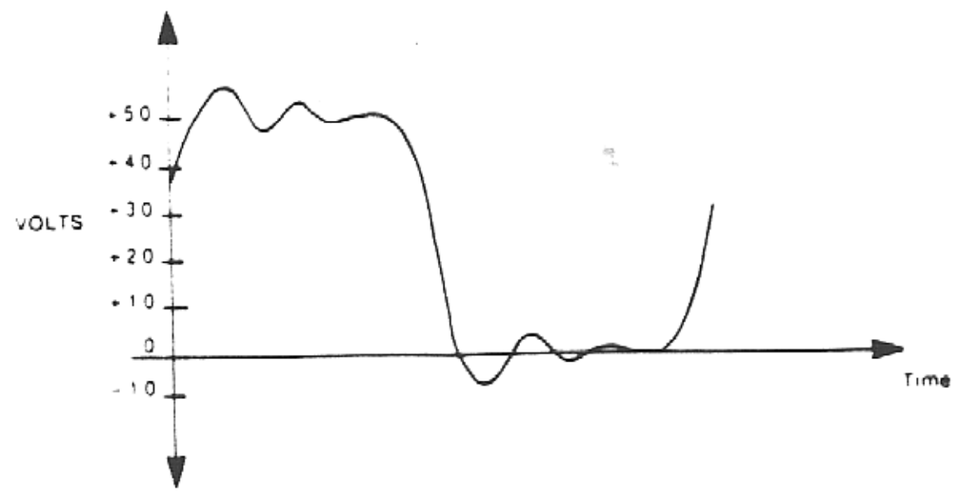


Figure 2. TYPICAL "RINGING" WAVEFORM from TTL INPUT

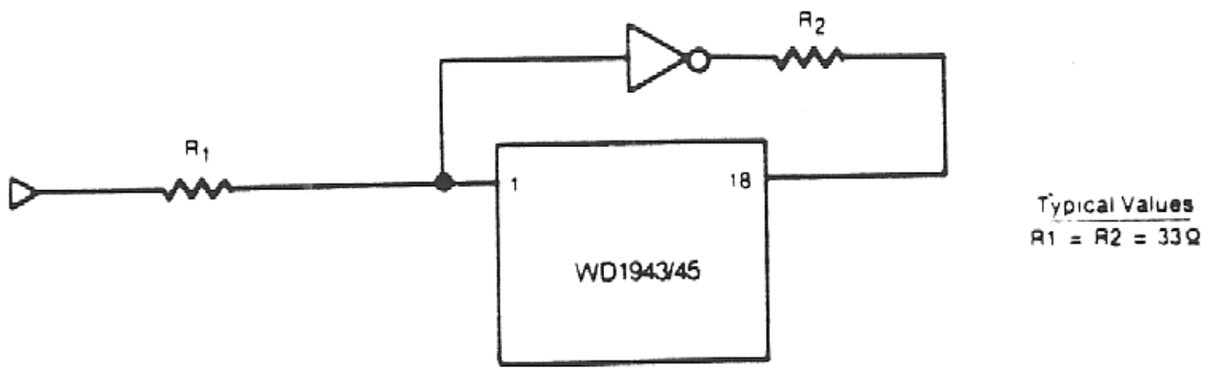


Figure 3. SERIES RESISTOR TO MATCH IMPEDANCE

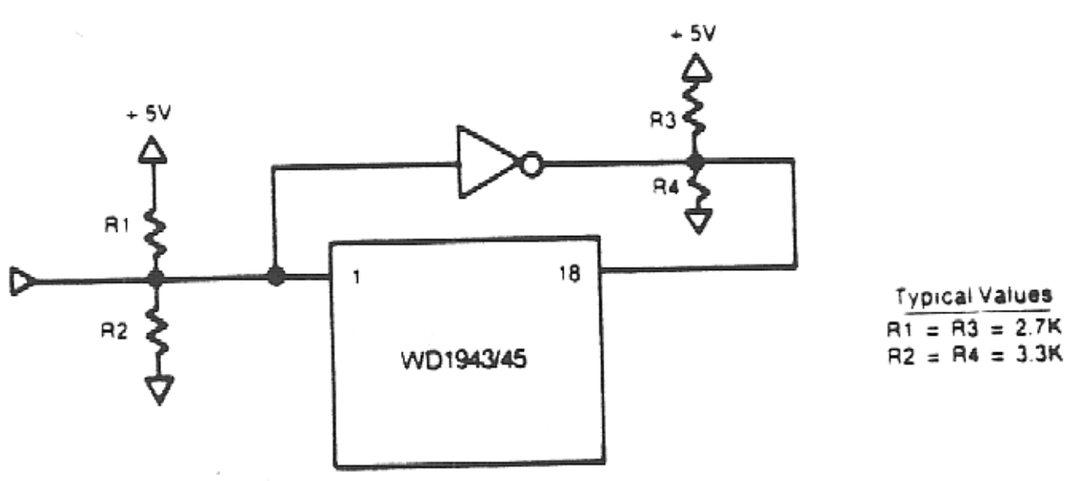


Figure 4. PULL-UP/PULL-DOWN RESISTORS TO MATCH IMPEDANCE

Figure 5. HIGH-SPEED DIODE TO CLAMP UNDERSHOOT